IN THE CLAIMS:

Please amend the claims as follows:

1. (Previously Presented) An electronic device, comprising:

an accelerator configured to accelerate cryptographic data processing operations, which accelerator comprises:

a first logical interface over which data to be processed is provided, and

a secure second logical interface over which cryptographic keys employed in processing data is provided, wherein the first logical interface and the secure second logical interface share a same physical interface, and said electronic device further comprises

a configuration register configured to indicate to the accelerator whether secure mode or normal mode is set by a processor, and configured to receive mode setting instructions from a protected application, wherein said processor is arranged in the electronic device, and

wherein the first logical interface is not accessible when data is transferred in the second logical interface.

2-3. (CANCELLED)

4. (Previously Presented) The device according to claim 1, wherein the configuration register further is configured such that it may be set in one of a plurality of possible encryption modes, and the accelerator is configured to operate in the encryption mode set in the register.

5. (CANCELLED)

6. (Previously Presented) The device according to claim 1, wherein the first logical interface of the accelerator is configured such that it is accessible by any application, while the secure second logical interface of the accelerator is configured such that it is accessible by protected applications only.

7. (Previously Presented) The device according to claim 6, wherein the protected applications are configured to prevent other applications from accessing the accelerator.

8. (Previously Presented) The device according to claim 6, wherein the protected applications are applications which are allowed to execute in the secure execution environment.

9. (Previously Presented) The device according to claim 1, further comprising:

storage circuitry comprising at least one storage area in which protected data relating to device security are located, and

wherein the processor is configured to be set in one of at least two different operating modes;

wherein the processor is given access to said storage area, in which said protected data are located, when a secure processor operating mode is set,

wherein the processor is denied access to said storage area when a normal processor operating mode is set; and

wherein the processor is capable of accessing the secure second logical interface of the accelerator, when the secure processor operating mode is set.

10. (Previously Presented) The device according to claim 9, wherein the processor is configured such that protected applications control the processor operation mode.

11. (Previously Presented) A mobile communication terminal comprising a device according to claim 1.

12. (Previously Presented) A device for acceleration of data processing operations, which device comprises:

a first logical interface over which data to be processed is provided; and

a secure second logical interface over which cryptographic keys employed in processing said data is provided, wherein the first logical interface and the secure second logical interface share a same physical interface, and

a configuration registered configured to indicate to the device whether secure mode or normal mode is set by a processor, and configured to receive mode setting instructions from a protected application, said processor being arranged in the device,

wherein the first logical interface is not accessible when data is being transferred in the second logical interface.

13-14. (CANCELLED)